REMARKS

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

The specification is amended to make minor editorial changes. A new title is added and labels are added to FIGS. 35 and 36.

Claims 1-20 are present in this application, claims 7-20 have been withdrawn from consideration. Claims 1 and 2 are amended by way of the present amendment.

Claims 1-6 stand rejected under 35 U.S.C. §112, second paragraph. Claims 3-5 stand rejected under 35 U.S.C. §112, first paragraph. Claims 1 and 6 stand rejected under 35 U.S.C. §102(e) over U.S. 6,342,715 (Shimizu et al.), and claims 2-5 stand rejected under 35 U.S.C. §103(a) over Shimizu et al. in view of U.S. 6,417,051 (Takebuchi).

The §112, first paragraph, rejection is respectfully traversed. As is known in this art, ion implantation is generally performed over the surface of a device. Masking is used to direct the impurities to particular area and to prevent impurities from entering other areas. In the present invention, a cell array area having memory cells and a peripheral area having transistors are implanted. As explained in the specification at page 20, line 30 - page 21, line 4, phosphorus is used to dope the floating gates of the cell array transistors and arsenic is doped into the gates of the peripheral area transistor gates. Also, the text on page 3, line 32 - page 4, line 4, and page 19, lines 20-22 explains how ions are implanted into the gate electrodes as the same time as the substrate to dope the gate electrodes and to form source and drain regions. One skilled in this art understands ion implantation of the respective areas happens in this manner. The text on page 17, lines 32-36 explains how ions are implanted into the cell array region and the peripheral region under different conditions to obtain desired

conductivity types and optimum impurity concentrations for the gate electrodes and for the source/drain regions.

The specification clearly supports claims 3-5. Moreover, claims 3-5 are original claims and constitute clear disclosure (see MPEP §608.01(l). Withdrawal of the §112, first paragraph, rejection is respectfully requested.

In response to the §112, second paragraph, rejection it has been clarified in claim 1 that the bottom layer of the floating gate and the bottom layer of the gate electrodes are maintained in self-alignment with the device isolation film. Also, the last phrase of claim 1 regarding impurities being doped under different conditions has been clarified, and claim 2 has been more broadly rewritten to state that the thicknesses of the transistors are different from each other. Claims 1-6 are believed to be in full compliance with §112, second paragraph, and withdrawal of this rejection is respectfully requested.

Turning to the §102/103 rejections, claim 1 recites the bottom layer of the floating gates of the non-volatile memory cells and the bottom layer of the gate electrodes of the transistors in the peripheral circuit being maintained in self-alignment with the device isolation insulating film, N type impurities doped into the gate electrodes of NMOS transistors and P type impurities doped in the gate electrodes of PMOS transistors in the peripheral circuit. As stated in the Office Action, Shimizu et al. was not found to disclose a peripheral circuit having an N type impurity doped into an NMOS transistor and a P type impurity doped into a PMOS transistor in the peripheral circuit (see page 8 of the Office Action). Accordingly, claim 1 is clearly patentably distinguishable over Shimizu et al. and withdrawal of the §102(e) rejection is respectfully requested.

Shimizu et al. appears to only suggest doping the gates of the peripheral transistors and the floating gates of the memory transistors with N type impurities. Shimizu et al.

contains no suggestion of the device of claim 1. As discussed in the specification, for example, on page 15, problems arise when one considers doping N and P type impurities.

Takebuchi, on the other hand, discloses a well-known transistor with a CMOS structure in a peripheral circuit. There is no suggestion of the structure of claim 1 where both the transistors in the peripheral and in the memory cell array have bottom layers in self-alignment with the device isolation insulating film, and N and P type impurities are doped into gate electrodes of NMOS and PMOS transistors, respectively, in the peripheral circuit. The disclosure of only the well-known CMOS of Takebuchi does not provide the necessary motivation to modify the structure of Shimizu et al. to include the transistors in the peripheral circuit having both N and P type impurities as recited in claim 1. Claim 1 is patentably distinguishable over a combination of Shimizu et al. and Takebuchi. and therefore is in condition for allowance.

It is respectfully submitted that the present application is in condition for allowance and a favorable decision to that effect is respectfully requested.

Respectfully submitted,
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